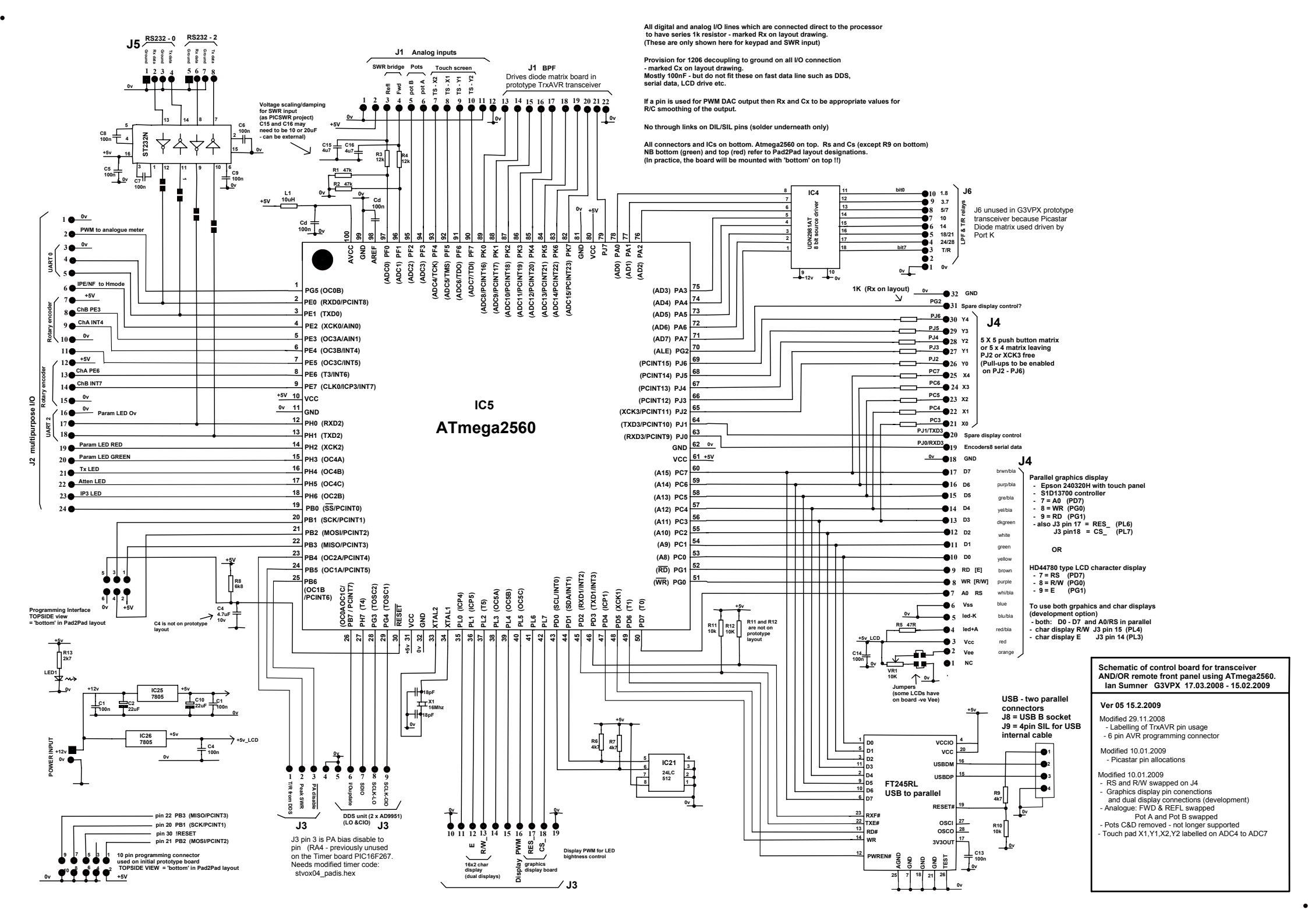
All digital and analog I/O lines which are connected direct to the processor to have series 1k resistor - marked Rx on layout drawing. (These are only shown here for keypad and SWR input)
Provision for 1206 decoupling to ground on all I/O connection - marked Cx on layout drawing. Mostly 100nF - but do not fit these on fast data line such as DDS, serial data, LCD drive etc.
If a pin is used for PWM DAC output then Rx and Cx to be appropriate values for R/C smoothing of the output.
No through links on DIL/SIL pins (solder underneath only)
All connectors and ICs on bottom. Atmega2560 on top. Rs and Cs (except R9 on bottom) NB bottom (green) and top (red) refer to Pad2Pad layout designations. (In practice, the board will be mounted with 'bottom' on top !!)
J5 RS232 - 0 RS232 - 2
J1 Analog inputs
SWR bridge Pots Touch screen
J1 BPF
Drives diode matrix board in prototype TrxAVR transceiver
Voltage scaling/damping for SWR input (as PICSWR project) C15 and C16 may need to be 10 or 20uF - can be external)
ST232N
IC4
UDN2981AT 8 bit source driver
J6
J6 unused in G3VPX prototype transceiver because Picastar Diode matrix used driven by Port K
LPF & T/R relays
J2 multipurpose I/O
UART 0
UART 2
Rotary encoder
IPE/NF to Hmode
ChB PE3
ChA INT4
ChA PE6
ChB INT7
Param LED Ov
Param LED RED
Param LED GREEN
Tx LED
Atten LED
IP3 LED
PWM to analogue meter
IC5
ATmega2560
1K (Rx on layout)
J4
5 X 5 push button matrix or 5 x 4 matrix leaving PJ2 or XCK3 free (Pull-ups to be enabled on PJ2 - PJ6)
Spare display control?
Spare display control
Encoders8 serial data
J4
Parallel graphics display
- Epson 240320H with touch panel
- S1D13700 controller
- 7 = A0 (PD7)
- 8 = WR (PG0)
- 9 = RD (PG1)
- also J3 pin 17 = RES_ (PL6)
J3 pin18 = CS_ (PL7)
OR
HD44780 type LCD character display
- 7 = RS (PD7)
- 8 = R/W (PG0)
- 9 = E (PG1)
To use both grpahics and char displays (development option)
- both: D0 - D7 and A0/RS in parallel
- char display R/W J3 pin 15 (PL4)
- char display E J3 pin 14 (PL3)
Programming Interface TOPSIDE view = 'bottom' in Pad2Pad layout
C4 is not on prototype layout
R11 and R12 are not on prototype layout
Jumpers (some LCDs have on board -ve Vee)
USB - two parallel connectors
J8 = USB B socket
J9 = 4pin SIL for USB internal cable
FT245RL USB to parallel
POWER INPUT
IC25 7805
IC26 7805
J3
J3 pin 3 is PA bias disable to pin (RA4 - previously unused on the Timer board PIC16F267. Needs modified timer code: stvox04_padis.hex
T/R from DDS
Peak SWR
PA disable
VCOupdate
SDO
SCK-LO
SCK-HO
DDS unit (2 x AD9951) (LO &CIO)
pin 22 PB3 (MISO/PCINT3)
pin 20 PB1 (SCK/PCINT1)
pin 30 !RESET
pin 21 PB2 (MOSI/PCINT2)
10 pin programming connector used on initial prototype board TOPSIDE VIEW = 'bottom' in Pad2Pad layout
16x2 char display (dual displays)
graphics display board
Display PWM for LED bightness control
Schematic of control board for transceiver AND/OR remote front panel using ATmega2560.
Ian Sumner G3VPX 17.03.2008 - 15.02.2009
Ver 05 15.2.2009
Modified 29.11.2008
- Labelling of TrxAVR pin usage
- 6 pin AVR programming connector
Modified 10.01.2009
- Picastar pin allocations
Modified 10.01.2009
- RS and R/W swapped on J4
- Graphics display pin conenctions and dual display connections (development)
- Analogue: FWD & REFL swapped Pot A and Pot B swapped
- Pots C&D removed - not longer supported
- Touch pad X1,Y1,X2,Y2 labelled on ADC4 to ADC7